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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,178	07/25/2000	Hiroki Nakamura	F98ED0762	7254

7590 12/03/2002

Junichi Mimura
OKI America Inc
Suite 555
1101 14th Street NW
Washington, DC 20005

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/625,178	NAKAMURA, HIROKI	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on th cover sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *21-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 27-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 10, 2002 has been entered.

Amendment

2. Amendment filed September 10, 2002 has been entered as Paper No. 16. Claims 1, 3, 4, 9-11, 13-16, 18-20, 27, 29 and 31-33 have been amended. Claims 1-33 are pending. Claims 21-26 have been withdrawn.

Response to Amendment

3. The amendment filed Sept 10, 2002 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "a peripheral area where an integrate circuit is not formed, the peripheral area surrounding the circuit area".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-20 and 27-33 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "a peripheral area where an integrate circuit is not formed, the peripheral area surrounding the circuit area" in the application as originally filed.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-20 and 27-33 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that all claims fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the specification filed July 25, 2000. In that paper, applicant has stated (corrected version) "A bonding pad 601 is formed in a circuit area...A frame-shaped fourth dummy pattern 600a is formed surrounding the bonding pad 601 in the circuit area", and this statement indicates that the invention is different from what is defined in the claim(s) because clearly a portion of the integrated circuit **is formed** in the dummy area.

While the amended claims recite: "**a peripheral area where an integrate circuit is not formed**".

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-4, 11-15, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha et al. (JP-10-270445) in view of Hosoda et al. (JP-08-181208) (all cited previously).

With respect to claim 1, as best understood by the examiner, Yamaha teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (10) having a circuit area (RA) where an integrated circuit is formed and a peripheral area, where an integrated circuit is not formed, surrounding the circuit area;

wiring patterns (12) formed on the substrate (10) in the circuit area;

a first dummy pattern (13) which is formed of the same material as the wiring pattern, formed in the dummy area;

a first insulating layer (14a) formed on wiring patterns (12) and the dummy pattern (13) of the semiconductor substrate (10);

a second insulating layer (14b) formed on the first insulating layer (14a) which is formed on the semiconductor substrate, wherein the second insulating layer (14b) is formed over the first

wiring pattern (12), and the second insulating layer (14b) is not formed over the first dummy pattern (13); and

a third insulating layer (14c) formed on the exposed first insulating layer (14a) and the second insulating layer (14b). (See Fig. 5).

Thus, Yamaha is shown to teach all the features of the claim with the exception of explicitly show that the dummy pattern (13) encompassing the circuit area (RA).

However, Hosoda teaches that the dummy patterns (14a) can be formed any where on a chip including surrounding the circuit pattern, hence peripheral area (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the dummy patterns (13) of Yamaha encompassing the circuit area (12) as taught by Hosoda to improve the planarity of the chip.

Regarding the circuit area and the peripheral area, it is well known that all semiconductor chip has circuit area where the IC is formed and the peripheral area surrounding the circuit.

Product by process limitation:

The expression "the width of the first (and third) dummy pattern is fixed by a concentration of solid content of the SOG (claims 3, 14 and 19); where a concentration of solid content of the SOG layer is around 5.2 wt% (claims 4, 10, 15 and 20); thermally planarized surface (claim 5)" are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA

1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that, the solid content of the SOG only is only **existed before** being deposited or process step, on the semiconductor substrate, as a semiconductor device, the SOG layer after being deposited and cures, final product, is **no longer contained 5.2 wt %** as claimed.

With respect to claim 2, the second insulating layer (14b) of Yamaha is a SOG layer.

With respect to claim 3, insofar as the device is concerned, the first dummy pattern (13) of Yamaha has a width.

With respect to claim 4, insofar as the device is concerned, the width of the first dummy pattern (13) of Yamaha is designed for various size including less than 1μm.

With respect to claim 11, the device of Lee also includes: a third dummy pattern (13e) formed in the dummy area between the first dummy pattern (13d) and the wiring patterns (12).

Since the dummy pattern (13) of Yamaha can be a single wide pattern (13) or multiple narrower patterns (13a-e), therefore, the second insulating layer (14b) can be eliminated from the surface of the multiple dummy patterns as shown in fig. 5.

With respect to claim 12, the width of the third dummy pattern (13e) of Yamaha appears to be almost the same as that of the first dummy pattern (13d).

With respect to claim 13, there is a distance between the first (13d) and third (13e) dummy pattern of Yamaha. Since the dummy patterns (13a-e) are not used for connecting circuit elements, their sizes and spacing distribution can be selected freely.

Further, the claimed distance between the first and third dummy patterns of "exceeds 0.9μm" does not appear to be critical.

Therefore, within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum spacing of the dummy lines. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation".

With respect to claim 14, insofar as the device is concerned, the second insulating layer (14b) of Yamaha is a SOG layer.

With respect to claim 15, insofar as the device is concerned, the second insulating layer (14b) of Yamaha is a SOG layer and each of the first (13d) and third (13e) dummy patterns of Yamaha. With respect to the size of the dummy patterns, the similar reason as that of claim 13 is also applied here.

With respect to claim 27, as best understood by the examiner, Yamaha teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (10) having a circuit area where an integrated circuit is formed and a peripheral area, where an integrated circuit is not formed, surrounding the circuit area;

wiring patterns (12s) formed on the substrate (10) in the circuit area (RA);

a dummy pattern (13) which is formed of the same material as the wiring pattern (12), formed in the dummy area (RB); and

an insulating layer (14b) formed above the semiconductor substrate (10), the insulating layer (14b) being formed over the wiring patterns (12), the insulating layer (14b) being formed outside the dummy pattern (13) but not being formed over the dummy pattern (13), and the insulating layer (14b) having a moisture absorbable characteristic. (See Fig. 5).

Thus, Yamaha is shown to teach all the features of the claim with the exception of explicitly show that the dummy pattern (13) encompassing the circuit area (RA).

However, Hosoda teaches that the dummy patterns (14a) can be formed any where on a chip including encompassing the wiring area (13) at the edge of the chip (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the dummy patterns (13) of Yamaha encompassing the wiring patterns (12s) as taught by Hosoda to improve the planarity of the semiconductor device.

Regarding the moisture absorbable characteristic, since the insulating layer (14b) of Yamaha is SOG, thus, the insulating layer (14b) of Yamaha inherently has a moisture absorbable characteristic.

With respect to claim 28, the insulating layer (14b) of Yamaha is a second insulating layer, the semiconductor device of Yamaha further comprises first (14a) and third (14c)

insulating layers formed on the substrate (10), the second insulating layer (14b) being located between the first insulating layer (14a) and the third insulating layer (14c).

Response to Arguments

7. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
November 29, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800